What is claimed is:

1. A method for shrinking a dimension of a gate, comprising;

providing a semiconductor structure;

forming a semiconductor gate on said semiconductor structure;

forming a first oxide layer on a surface of said semiconductor gate and said semiconductor structure, wherein said thickness of said first oxide layer is in accordance with the thickness of a second oxide layer above a dummy wafer; and

removing said first oxide layer, wherein a etching solution is used to remove said first oxide layer.

2. The method of claim 1, wherein said semiconductor structure comprises a semiconductor substrate and a plurality of isolation zones therein.

3. The method of claim 2, wherein said semiconductor gate comprises a polysilicon layer and a gate oxide layer thereon.

4. The method of claim 3, wherein comprises a plurality of ions doped therein.

5. The method of claim 1, wherein said first oxide layer comprises utilizing a method of thermal oxidation to deposit.

6. The method of claim 1, wherein said first oxide layer comprises utilizing a method of conformal to deposit.

7. The method of claim 1, wherein said etching solution comprises a hydrofluoric acid solution.

8. The method of claim 7, wherein said hydrofluoric acid solution comprises a DHF solution (HF in deionized water).

9. The method of claim 1, wherein said etching solution comprises a BOE solution (Buffered Oxide Etch).

10. The method of claim 9, wherein said BOE solution comprises a HF/NH_4F buffered solution.

11. A method for shrinking a dimension of a gate, comprising;
providing a semiconductor substrate;
forming a first oxide layer on said semiconductor substrate;
forming a polysilicon layer on said first oxide layer;
forming a photoresist layer on said polysilicon layer;
patterning said photoresist layer;

etching a portion of said polysilicon layer and said first oxide layer until a portion of said semiconductor substrate is exposed, wherein said patterned photoresist layer is utilized as a mask;

removing said patterned photoresist layer;

performing an oxidation on a surface of said polysilicon layer, said first layer and said semiconductor substrate to form a second oxide layer on said surface of said polysilicon layer, said first oxide layer and said semiconductor substrate, wherein said thickness of said second oxide layer is in accordance with the thickness of a third oxide layer above a dummy wafer; and

removing said second oxide layer, wherein a etching solution is used to remove said second oxide layer.

12. The method of claim 11, wherein said second oxide layer comprises utilizing a method of thermal oxidation to deposit.

13. The method of claim 11, wherein said second oxide layer comprises utilizing a method of conformal to deposit.

14. The method of claim 11, wherein said etching solution comprises a hydrofluoric acid solution.

15. The method of claim 14, wherein said hydrofluoric acid solution comprises a DHF solution (HF in deionized water).

16. The method of claim 11, wherein said etching solution comprises a BOE solution (Buffered Oxide Etch).

17. The method of claim 16, wherein said BOE solution comprises a HF/NH_4F buffered solution.